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Comparative Evaluation of Two-Dimensional Interfacial Control Layers in Memristors

Peimeng Wang[1*]

[1] Beijing Institute of Technology, Beijing, China

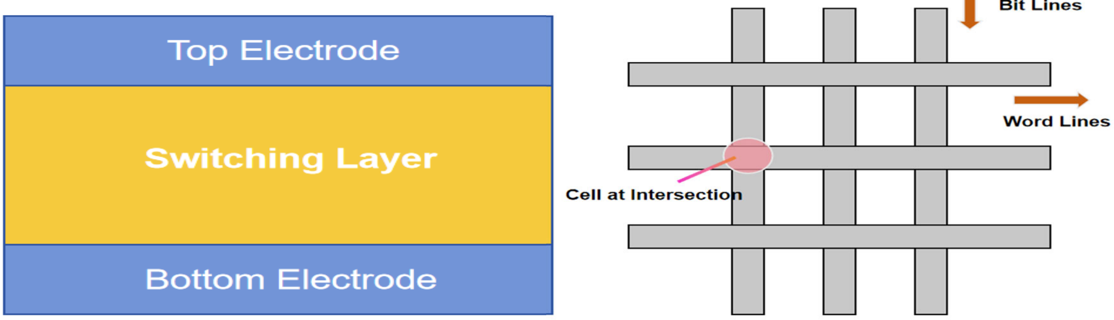
*E-mail: u202342003@xs.ustb.edu.cn

Abstract. Two dimensional(2D) interfacial and tunneling layers provide a compact route to stabilizing and scaling memristors. This review compares four representative 2D families: graphene and graphene oxide, hexagonal boron nitride, transition metal dichalcogenides, and MXenes. The research describes how these layers regulate charge injection and ion transport, and how those effects map to device and array metrics. Common benefits include lower programming voltage and energy, tighter variability, improved analog update linearity, and mitigation of sneak paths, with trade offs in film transfer, long term stability, and selector integration. The research highlights three practical design levers: layer thickness, contact and work function alignment, and defect or surface termination control, and the research offers concise guidelines for engineering energy efficient, reliable, crossbar compatible memristive systems.

Keywords: Two dimensional materials, Interfacial and tunneling layers, Memristor scaling, Charge injection and ion transport, Crossbar arrays.

1. Introduction

Memristors are two terminal devices whose resistance can be programmed and retained, which makes them promising for nonvolatile memory, in memory computing, and neuromorphic hardware[1]. Their compact crossbar integration together with analog conductance tunability offers a route to lower data movement energy and to hardware neural networks that relax the von Neumann bottleneck[2]. Core device metrics include set and reset voltage and energy, on off ratio, switching speed, analog linearity and symmetry, multilevel capacity, and variability, along with endurance, retention, and immunity to read disturb that together determine reliability in practice[3]. As shown in Figure 1, a typical device uses a top electrode, a switching layer, and a bottom electrode, and large scale arrays adopt a crossbar that addresses each cell at line intersections.

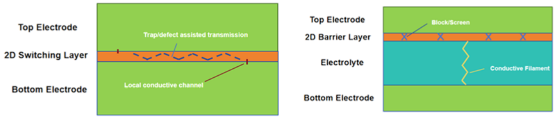


(a)Memristor (MIM) - Side View (b)Memristor Crossbar – Top View

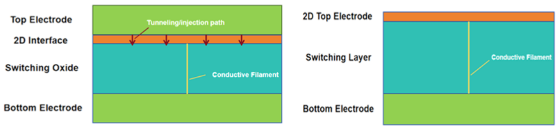
Figure 1. Schematic Diagram of a Memristor

At the array level, selector nonlinearity, wire resistance induced voltage drop, yield, and spatial uniformity determine the usable crossbar size and the accuracy of in memory multiply and accumulate operations[4]. Beyond dense information storage, memristor arrays enable analog matrix vector multiplication for deep learning accelerators and also support flexible or skin integrated edge sensing and compute platforms with tight power budgets[5].

Conventional device stacks span transition metal oxides, chalcogenides, electrochemical systems, organics, and ferroelectrics, where materials choice, electrode selection, doping strategy, and interfacial layers jointly set switching mechanism, forming voltage, variability, and retention trade offs[6]. Two dimensional materials add atomic level thickness, atomically sharp van der Waals interfaces, mechanical flexibility, and rich surface chemistry that together open new ways to control defects, ion transport, and the underlying switching physics[7]. In practical architectures, such two dimensional layers can act as switching media, interfacial and tunneling control layers, diffusion barriers, or even electrodes, which can improve uniformity, suppress leakage, and reduce stochastic filament growth at scale[8]. Figure 2 summarizes these four roles of two dimensional layers within memristors and highlights their typical transport pathways and blocking effects.



(a) 2D as Switching Layer (b) 2D as Diffusion Barrier



(c) 2D as Interface/Tunneling Layer (d) 2D as Electrode

Figure 2. The Role of Two-Dimensional Materials in Memristors

In multi terminal memtransistors, a two dimensional semiconducting channel together with a gate offers extra control over conductance states, linearity, and volatility, which is attractive for analog synapses and neuron like dynamics[9]. Emerging two dimensional van der Waals ferroelectrics further enable polarization controlled resistive switching at low voltage with nondestructive readout and strong retention, pointing to compact and energy efficient building blocks for future computing systems[10].

Building on this background, this paper elucidates the specific roles and applications of diverse two-dimensional (2D) materials employed as interfacial and tunneling modulation layers in memristors, systematically analyzes their impacts on device-level performance metrics, reliability, and array-level performance, and conducts a comparative analysis across these materials.

2. Role of 2D Interfacial and Tunneling Control Layers in Memristors

Two dimensional materials used as interfacial and tunneling control layers give angstrom level control over charge injection and ion motion, aided by atomically flat van der Waals surfaces that reduce roughness and parasitic diffusion. By aligning bands and tailoring dipolar and defect chemistry, they tune the Schottky barrier and steer the tunneling mode from direct to Fowler Nordheim, which lowers switching voltage and energy[11]. As shown in Figure 3, the introduction of a two dimensional interfacial layer tailors the effective barrier, making it thinner and easier to penetrate, which results in a lower set voltage and smoother conductance updates compared with devices without such a layer.

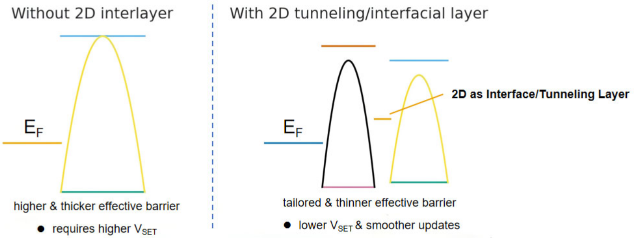


Figure 3. Energy band diagrams: without vs. with a 2D interfacial/tunneling layer

As ultra thin diffusion and redox buffers, these films confine oxygen vacancy and metal filament growth both laterally and vertically, limiting overgrowth and overshoot while promoting uniform conductive paths. In charge trap type stacks, two dimensional dielectrics and functionalized sheets provide tunable trap spectra that support smooth, incremental conductance updates with good linearity and symmetry[12]. Together these effects yield lower forming and set thresholds, higher on off ratios, narrower parameter spreads, stronger endurance and retention, and smaller cycle to cycle and device to device variation. At the array scale they increase current voltage nonlinearity for sneak path suppression, expand read margins, and enable more linear and symmetric weight updates for in memory computing. Representative families including graphene and graphene oxide, hexagonal boron nitride, transition metal dichalcogenides such as MoS2, and MXenes offer complementary levers across these objectives, making two dimensional interfacial control layers a practical path to scalable, energy efficient, and reliable memristive technology.

3. Graphene Family Interlayers (Graphene, Graphene Oxide, Rgo)

3.1 Interfacial and tunneling mechanism

As a van der Waals and atomically flat sheet, graphene minimizes roughness induced field spikes at the metal dielectric contact and sets a well defined injection barrier[13]. P type or n type doping and work function tuning then shift that barrier in a controlled way.

In graphene oxide and reduced graphene oxide, oxygenated groups and defects create a dense and shallow trap landscape that enables trap assisted tunneling and controllable filament nucleation and annihilation in the adjacent dielectric[14]. In practice, an approximately 0.5 to 3 nanometer graphene oxide or reduced graphene oxide film acts as an ultrathin tunneling spacer and diffusion throttle that slows silver, copper, and oxygen migration, narrows the filament cross section, and adds a small series resistance that damps overshoot during the set process, which makes updates smoother and more reproducible[15]. As shown in Figure 4, the insertion of a graphene oxide interlayer increases the space charge limited conduction exponent compared with a single Ga2O3 device, especially in the square law and high field regions, indicating stronger trap controlled transport and more efficient charge modulation.

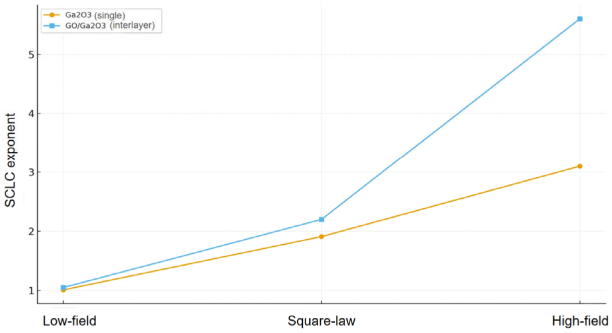


Figure 4. Effect of GO interlayer on SCLC exponents

3.2 Key performance implications

At the device level, graphene based interfacial layers combine atomic scale planarity with a tunable work function achieved through doping and functional groups and with controllable defect and trap densities found in graphene oxide and reduced graphene oxide. When used as ultrathin tunneling and barrier membranes with thickness approximately 0.5 to 3 nanometer, typical observations include reduced set voltages from below 1 volt to about 1.5 volt while maintaining on off ratios of ten to the third to ten to the fifth. Oxygen containing sites in graphene oxide promote more reproducible filament formation and annealing and narrow cycle to cycle switching dispersion. Graphene electrodes lower series resistance and local Joule heating, which enables smoother analog weight updates. Conductive graphene suppresses hot spots. Graphene oxide throttles ion flux and thereby reduces write energy. Partial modulation of conductive filaments by graphene oxide and reduced graphene oxide enables stable intermediate multilevel states. With respect to analog linearity and symmetry, interfacial trap assisted tunneling together with small series resistance yields smoother and more symmetric conductance potentiation and depression with reduced pulse to pulse variability.

For variability and reliability in carbon based resistive switching, replacing pure metal filaments with carbon filaments or with carbon modulated silver and copper filaments shifts the active region to a carbonaceous matrix and achieves retention of ten to the fifth to ten to the sixth seconds and endurance of ten to the sixth to ten to the seventh cycles. Acting as a diffusion throttle valve, graphene oxide and reduced graphene oxide suppress overgrowth and short type failures and improve reset completeness. A smoother interface and a lower local electric field further decrease the probability of random hard breakdown. As a result, diffusion throttling combined with planar interfaces reduces device to device dispersion [15].

At the array level, inter array update uniformity is improved and compatibility with large area printing and chemical vapor deposition processes increases yield. The enhanced symmetry also helps mitigate IR drop amplified write errors in large and deep arrays.

4. Hexagonal boron nitride (h-BN) tunneling and guard layers

4.1 Interfacial and tunneling mechanism

Few layer h-BN with a bandgap of about 5.9 eV serves as a robust and uniform tunneling barrier that can convert volatile and filament dominated switching into barrier modulated or confined pathway switching. Engineered point defects such as VB vacancies introduce controllable conduits for trap assisted tunneling, and the choice of metal contact to h-BN sets a predictable Schottky and tunneling profile[16]. As shown in Figure 5, increasing the h-BN thickness correlates with a reduction in the extracted effective mass, which is consistent with a transition toward a more ideal and thickness controlled tunneling barrier.

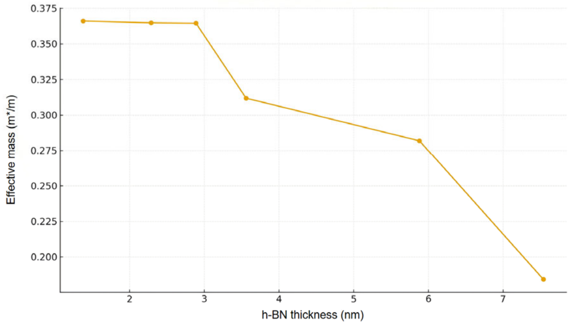


Figure 5. h-BN effective mass vs thickness (tunneling)

In hybrid stacks composed of oxide, h-BN, and oxide, the h-BN layer functions as a guard that suppresses uncontrolled metal or anion diffusion and localizes the active region at a designed plane. This interfacial control improves switching uniformity and stabilizes the active pathway during repeated cycling, which supports lower variability and more reliable updates at practical bias levels .

4.2 Interfacial and tunneling mechanism

At the device performance level, h-BN offers a wide bandgap of about 5.9 eV and an atomically flat surface, which makes it an excellent few layer tunneling barrier with a thickness of about 0.7 to 3 nanometer or a gateable spacer [17]. In metal to h-BN to metal junctions and in compositestacks such as oxide then h-BN then oxide, thresholds below 1 volt with clean turn on and turn off are commonly observed, and the uniform barrier suppresses overshoot and lowers the write energy. By modulating trap occupancy or nanoscale conduction channels within few layer h-BN, stable multilevel states can be achieved. Adjusting growth and defect chemistry, electrode metals, and the number of layers enables a tunable trade off between threshold steepness and analog tuning range.

For variability and reliability, the chemical inertness and the relatively high thermal conductivity of h-BN mitigate hot spots and runaway diffusion, which reduces drift in the high resistance state and the low resistance state, strengthens high temperature retention, and improves cycle to cycle consistency. Through deliberate vacancy engineering, careful metal selection, and multilayer stacking, filament overgrowth and stuck on conduction can be avoided. A smoother interface and a controlled local electric field further lower the probability of hard breakdown, and diffusion throttling combined with planar interfaces reduces device to device variation.

At the array level, h-BN acts as a selector like threshold barrier that suppresses sneak path currents and stabilizes write and verify operation[18]. Its insulating nature facilitates co integration as a uniform protective interlayer beneath the top electrode, and inserting h-BN improves analog linearity and write symmetry while yielding better device to device uniformity across arrays. The controllable uniformity of few layer h-BN further enhances consistency and yield, and its selector like behavior helps mitigate write errors amplified by IR drop in large and deep crossbar arrays.

5. Transition-metal dichalcogenides as engineered interlayers

5.1 Interfacial and tunneling mechanism

Transition metal dichalcogenides provide phase tunability between the semiconducting two H phase and the metallic one T phase, together with vacancy and band edge control at van der Waals interfaces [19]. As interlayers with thickness of about one to five nanometer, they pin the filament root at a designed plane and set a controlled Schottky and tunneling barrier for electron injection, while trap planes support analog conductance changes under short pulse trains. As shown in Figure 6, the paired pulse facilitation index decreases with increasing pulse interval, which is consistent with trap mediated short term plasticity enabled by a TMD interlayer.

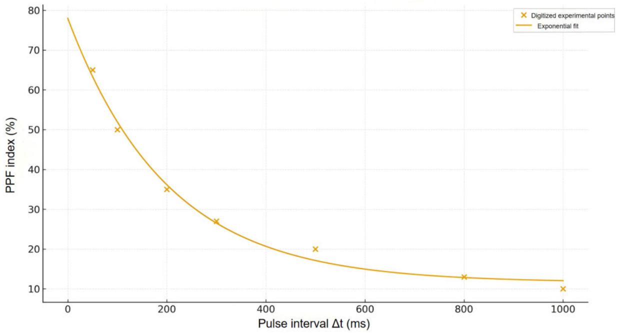


Figure 6. MoS_2 memristor short-term plasticity: PPF vs interval

Phase and defect engineering such as local one T patches and sulfur vacancies tailors the local energy landscape so that conductance updates proceed in small and repeatable increments rather than abrupt jumps [20]. This behavior improves write symmetry and reduces pulse to pulse variability in analog tuning.

5.2 Key performance implications

For device performance, transition metal dichalcogenides provide selectable semiconducting and metallic phases, chalcogen vacancies, and clean van der Waals interfaces [20]. As interfacial layers with thickness of about one to five nanometer, they can pin filament roots, tune the Schottky barrier, or offer a charge trapping plane that enables incremental analog conductance control. Using molybdenum disulfide as the interlayer commonly results in set voltages below one volt and on off ratios of ten to the third to ten to the sixth, which is attributed to root pinning and smoother barrier modulation as well as reduced device to device variability. For analog linearity and multilevel operation, phase and defect assisted trap dynamics allow more linear weight updates and reusable multilevel states, which is favorable for on chip learning.

With respect to variability and reliability, transition metal dichalcogenides decouple the active region from rough electrodes and suppress uncontrolled oxygen and metal migration, thereby narrowing the cycle to cycle switching distribution. When diffusion is constrained away from rough electrodes, thermal and environmental stability improves. By confining the filament cross section and limiting lateral branch growth, these materials also reduce random telegraph noise in the low resistance state.

At the array level, transition metal dichalcogenide interlayers are repeatedly used to enhance update linearity and to enable multiphysics coupling, which can partially mitigate voltage drop and improve bit wise addressing in deep crossbars, benefiting sensing and computing integration and sparse training schemes. Two dimensional or mixed dimensional stacks such as molybdenum disulfide combined with h-BN further improve weight update symmetry and reduce per update energy at the array level.

6. MXenes as interfacial modifiers and quasi-tunneling layers

6.1 Interfacial and tunneling mechanism

MXenes are metallic two dimensional carbides and nitrides whose surface terminations O, OH, and F establish interfacial dipoles and tune the work function[21]. A nanometer scale MXene sheet at the electrode to dielectric interface acts as a potential step and current spreader that seeds controlled filament nucleation, passivates deep traps at the contact, and introduces a gentle series resistance that tempers current surges[21]. As shown in Figure 7, a fully etched MXene contact turns on near about one volt and sustains higher current at the same bias compared with a partially etched MXene contact, which indicates a lower effective injection barrier and more efficient current spreading.

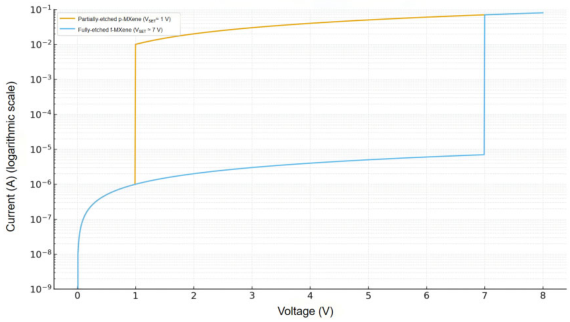


Figure 7. MXene interlayer tuning of threshold

When flakes are embedded in the dielectric, their terminations create a distributed and shallow trap network that supports analog conduction, and the overall effect depends sensitively on termination control and oxidation state[22].

6.2. Key performance implications

In terms of device performance, MXenes are metallic two dimensional carbides and nitrides with surface terminations O, OH, and F whose work function can be tuned by termination induced interfacial dipoles[23]. When used as a nanoscale interfacial layer or blended with the dielectric, they can lower the set threshold and tighten variability. The combination of more uniform nucleation sites and a controlled series resistance often leads to reduced programming energy and improved linearity of analog weight updates. The commonly observed decreases in set threshold and programming energy upon MXene insertion are attributed to barrier alignment and current homogenization.

Regarding reliability and variability, the surface chemistry is a double edged sword. Appropriate terminations can passivate traps and stabilize filaments, enabling more linear and symmetric updates and tighter cycle to cycle dispersion. Uncontrolled oxidation or moisture uptake can raise leakage and degrade retention. Post treatments, encapsulation, and organic inorganic hybrid matrices have pushed endurance to ten to the fifth to ten to the sixth cycles and enabled retention lasting weeks or longer under elevated temperatures.

At the array scale, MXene interlayers through hybridization with the active dielectric can show threshold like behavior that suppresses sneak leakage. Their tunable work function also facilitates wafer level barrier alignment, which reduces cell to cell spread during incremental programming, while solution processed low temperature fabrication supports high yield. These combined effects are advantageous for programming deep arrays under voltage drop constraints.

7. Cross-material comparison and design guidance

For set and reset behavior and analog linearity, when sub one volt clean threshold operation is the priority, h-BN and many TMD interlayers are generally robust, while the graphene family stands out for suppressing variability and delivering smooth analog updates with process friendly integration, and MXenes are attractive when work function engineering and trap passivation need to be combined with low programming energy[14]. As summarized in Figure 8, the normalized comparison highlights these trends across threshold, on off ratio, endurance, retention, variability, and update linearity.

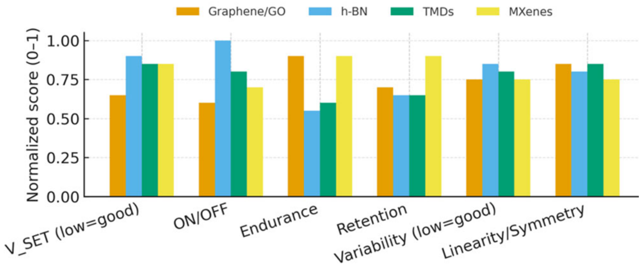


Figure 8. Qualitative, normalized performance comparison across 2D interfacial layers

In reliability oriented use, h-BN benefits from high thermal conductivity and chemical stability, the graphene family provides diffusion throttling and interfacial smoothing, MXenes can match these outcomes when surface terminations are tightly controlled and encapsulation is applied, and TMDs gain from phase and defect engineering that mitigates drift and noise[18].

Table 1. 2D interfacial layers comparative table

Metric	**Graphene / GO / rGO**	**h-BN**	**TMDs (e.g., MoS2/WS2)**	**MXenes (e.g., Ti3C2Tx)**
SET/Threshold voltage (V)	0.2–2	<1 (often 0.2–1)	0.1–1.2	0.1–1
ON/OFF ratio	10^2–10^6	10^4–10^8	10^3–10^7	10^3–10^6
Endurance (cycles)	10^4–10^7	10^2–10^4 (array); up to ~10^6 (device)	10^2–10^7	10^5–10^7
Retention (s)	≥10^4–10^5	≥2×10^4	10^4–10^5	≥10^5
Programming energy (per event)	pJ-class (device-dependent)	sub-pJ to pJ (arrays)	sub-pJ to pJ (arrays)	pJ-class (reports)
Variability (c2c / d2d)	often ≤20% with GO/rGO engineering	often ≤10–30% in arrays	often ≤10–30% in arrays	often ≤20% with interface tuning
Weight-update linearity / symmetry	Improved via GO defect/thickness grading	Good via atomically uniform tunneling barrier	Tunable via phase (2H↔1T), gating, heterojunctions	Tunable via terminal groups (–O/–OH/–F) & interfacial dipoles
Array demonstrations	Crossbar arrays; multi-level states; low-voltage write	1T1R/1S1R arrays; CMOS BEOL integration shown	4×4–10×10 arrays; pJ–fJ programming; training demos	Synaptic arrays; stable updates; integration-friendly
Primary role as interfacial/tunneling layer	Diffusion barrier / trap-rich ultrathin tunnel layer	Atomically thin, wide-gap tunneling barrier	Engineered barrier/trap layer; vdW heterointerfaces	Conductive interlayer with tunable work function

At the array level, graphene and many TMDs often yield better linearity and symmetry for gradient based in array learning, the thresholding of h-BN helps suppress sneak paths, and MXenes with tunable work function and solution compatible processing support large scale integration and yield[21]. Table 1 compiles practical metric ranges by material class and links them to the primary role of each interfacial or tunneling layer for design selection.

8. Conclusion

This study delivers an in depth analysis of the roles of four two dimensional material families used as interfacial and tunneling modulation layers in memristors. By clarifying how each material class interacts with electrodes and dielectrics, the work links interfacial physics to device and array outcomes. The comparative synthesis yields actionable guidance: match thickness to the intended transport regime, align contact work functions, and engineer defects or terminations to stabilize ion and charge pathways. Applied together, these levers lower set thresholds and energy, tighten variability, strengthen endurance and retention, and improve linear and symmetric weight updates, paving the way for reliable and crossbar compatible architectures.

References

[1] Thakkar P, Gosai J, Gogoi H J, et al. From fundamentals to frontiers: a review of memristor mechanisms, modeling and emerging applications[J]. Journal of Materials Chemistry C, 2024, 12(5): 1583-1608.

[2] Xiao Y, Jiang B, Zhang Z, Ke S, Jin Y, Wen X, Ye C. A review of memristor: material and structure design, device performance, applications and prospects. Sci Technol Adv Mater. 2023 Feb 28;24(1):2162323.

[3] Qin F, Zhang Y, Song H W, et al. Enhancing memristor fundamentals through instrumental characterization and understanding reliability issues[J]. Materials Advances, 2023, 4(8): 1850-1875.

[4] Zhou, H., Li, S., Ang, KW. et al. Recent Advances in In-Memory Computing: Exploring Memristor and Memtransistor Arrays with 2D Materials. Nano-Micro Lett. 16, 121 (2024)

[5] Xu J, Luo Z, Chen L, et al. Recent advances in flexible memristors for advanced computing and sensing[J]. Materials Horizons, 2024, 11(17): 4015-4036.

[6] Panisilvam J, Lee H Y, Byun S, et al. Two-dimensional material-based memristive devices for alternative computing[J]. Nano Convergence, 2024, 11(1): 25.

[7] Park S, Naqi M, Lee N, et al. Recent Advancements in 2D Material-Based Memristor Technology Toward Neuromorphic Computing[J]. Micromachines, 2024, 15(12): 1451.

[8] Zhang S, Tao Y, Qin S, et al. Memristors based on two-dimensional h-BN materials: synthesis, mechanism, optimization and application[J]. npj 2D Materials and Applications, 2024, 8(1): 81.

[9] Deng W, Yan X, Wang L, et al. Two-dimensional materials based memtransistors: Integration strategies, switching mechanisms and advanced characterizations[J]. Nano Energy, 2024, 128: 109861.

[10] Du J, Sun B, Yang C, et al. Ferroelectric memristor and its neuromorphic computing applications[J]. Materials Today Physics, 2025, 50: 101607.

[11] Kaniselvan, M., Jeon, YR., Mladenović, M. et al. Mechanisms of resistive switching in two-dimensional monolayer and multilayer materials. Nat. Mater. 24, 1346–1358 (2025).

[12] Rehman M M, Samad Y A, Gul J Z, et al. 2D materials-memristive devices nexus: From status quo to Impending applications[J]. Progress in Materials Science, 2025: 101471.

[13] Walters B, Jacob M V, Amirsoleimani A, et al. A review of graphene-based memristive neuromorphic devices and circuits[J]. Advanced Intelligent Systems, 2023, 5(10): 2300136.

[14] Patil, Dr.Snehal & Pawar, Omkar & Dongale, Dr. T. & Chang, Sehui & Lim, Sooman & Song, Young. (2024). Recent advancements in carbon-based materials for resistive switching applications. Carbon. 228. 119320. 10.1016/j.carbon.2024.119320.

[15] Yang F, Liu Z, Ding X, et al. Carbon-based memristors for resistive random access memory and neuromorphic applications[J]. Chip, 2024, 3(2): 100086.

[16] Nirmal K A, Kumbhar D D, Kesavan A V, et al. Advancements in 2D layered material memristors: unleashing their potential beyond memory[J]. npj 2D Materials and Applications, 2024, 8(1): 83.

[17] Roldan J B, Maldonado D, Cantudo A, et al. Conductance quantization in h-BN memristors[J]. Applied Physics Letters, 2023, 122(20).

[18] Qin S, Tao Y, Hu T, et al. Advances in two-dimensional heterojunction for sophisticated memristors[J]. Materials Today Physics, 2024, 41: 101336.

[19] Kwon K C, Baek J H, Hong K, et al. Memristive devices based on two-dimensional transition metal chalcogenides for neuromorphic computing[J]. Nano-Micro Letters, 2022, 14(1): 58.

[20] Tong W, Liu Y. Recent progress of layered memristors based on two-dimensional MoS2[J]. Science China Information Sciences, 2023, 66(6): 160402.

[21] Teixeira H, Dias C, Silva A V, et al. Advances on MXene-based memristors for neuromorphic computing: a review on synthesis, mechanisms, and future directions[J]. ACS nano, 2024, 18(33): 21685-21713.

[22] Lv L, Zhang P, Yang X, et al. Novel 2D MXene-based materials in memristors: Fundamentals, resistive switching properties and applications[J]. Surfaces and Interfaces, 2024, 44: 103678.

[23] Hota M K, Pazos S, Lanza M, et al. A review of MXene memristors and their applications[J]. Materials Science and Engineering: R: Reports, 2025, 164: 100983.