ISSN:2790-1688 Volume-14-(2025)

Peak Current Mode Controlled Four-Phase DC-DC Converter with Fast Load Transient Response

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Abstract. With the increasing demand for dynamic performance of power management integrated circuits (PMICs) in 5G portable devices, this paper proposes a peak current mode (PCM) controlled four-phase parallel DC-DC converter to enhance system stability and load dynamic response capability. By introducing inductor current feedback and ramp compensation, the risk of subharmonic oscillation is eliminated. Meanwhile, the four-phase interleaved topology (90° phase difference) significantly reduces I^2R losses and achieves current ripple cancellation; a Type II compensation network designed based on the small-signal model realizes a bandwidth of 90kHz and a phase margin of 40°. Simplis simulation verification shows that the output voltage stabilizes at 1V under steady state, and the currents of each phase are evenly shared; when the load steps by ±5A, the transient deviation of the output voltage is suppressed to 50mV, with a recovery time of 200μs.

Keywords: Load transient, peak current, DC-DC converter.

1. Introduction

With the advent of the 5G era, portable devices such as tablets, mobile phones, and laptops have become increasingly popular. Power management integrated circuits (PMICs) are indispensable key components in these portable electronic devices, ensuring stable operation and efficient energy consumption management. DC-DC switching converters are a common type of PMIC, often used to power portable computing devices. In this context, fast dynamic response under a wide load range is crucial for PMICs [1-3].

Currently, there are two classic control methods for switching DC-DC converters: Voltage Mode Control (VMC) and Current Mode Control (CMC). VMC relies on the adjustment of the voltage feedback loop and lacks real-time control of the inductor current, resulting in slow response to input voltage changes and sudden load variations [4]. In contrast, CMC adds a dual-loop circuit with an inductor current feedback circuit, featuring good voltage regulation and transient response. However, when the pulse width modulation (PWM) duty cycle exceeds 50%, subharmonic oscillation occurs, necessitating the addition of slope compensation in the control loop [5].

Multi-phase parallel DC-DC converters can significantly reduce I^2R losses in high-current scenarios [6]. In high-current applications, a single-phase converter bears the entire load current, and even with a small resistance R, the loss I^2R is substantial due to the large current I. Multi-phase parallel operation distributes the load current evenly, greatly reducing I^2R losses compared to single-phase converters.

CMC control offers core advantages for multi-phase DC-DC converters. The CMC controller includes multiple independent current loops, each sampling the inductor current of the corresponding phase in real time, comparing the sampled current with a reference signal to generate an error signal, which is then used to directly adjust the duty cycle of the phase's PWM after passing through a compensator. Thus, when the current of a phase is too high or too low, the current loop immediately adjusts the duty cycle of that phase to make its current approach I/4, achieving automatic current balancing [7]. Meanwhile, CMC employs cycle-by-cycle current limiting, comparing the sampled peak inductor current with a current limit threshold in each switching cycle. When the current exceeds the threshold, the PWM pulse of that phase is immediately interrupted, realizing automatic current protection [8].

Therefore, this paper proposes a Peak Current Mode Control (PCM) four-phase parallel DC-DC converter. It introduces fast inductor current feedback through current sampling to achieve rapid

inductor current response and current balancing among phases; voltage compensation ensures stable output voltage and eliminates steady-state voltage errors. Based on small-signal modeling under the switch averaging method, the loop bandwidth and phase margin are compensated to an appropriate range. Finally, Simplis simulation verifies the system circuit design.

2. Control Loop Design

The four-phase parallel DC-DC converter adopted in this paper is composed of multiple single-phase BUCK circuits cascaded in an interleaved manner. As shown in Fig. 1, the four-phase parallel DC-DC converter consists of components such as inductors, capacitors, power switches, and MOS transistors. When four single-phase BUCK circuits are cascaded in an interleaved manner, the PWM waveform of each phase is delayed by T/4, with the phase controlled at 90°. At this time, the inductor current of each phase of the four-phase parallel DC-DC converter is consistent with the PWM control waveform, and the peaks and valleys of the inductor currents of different phases cancel each other out, reducing the output voltage ripple. The converter is composed of a power stage and a feedback network. The power stage includes switching elements composed of PMOS and NMOS transistors, as well as an output filter composed of inductor elements and filter capacitors. The output voltage *Vo* is generated by the power stage circuit. *Vo* is compared with the reference voltage Vref to generate an error signal, which is compared with the ramp signal and inductor current. Finally, the duty cycle D is defined by an SR latch. The duty cycle D controls the on-time and off-time of the transistors to achieve negative feedback regulation of the output voltage *Vo*.

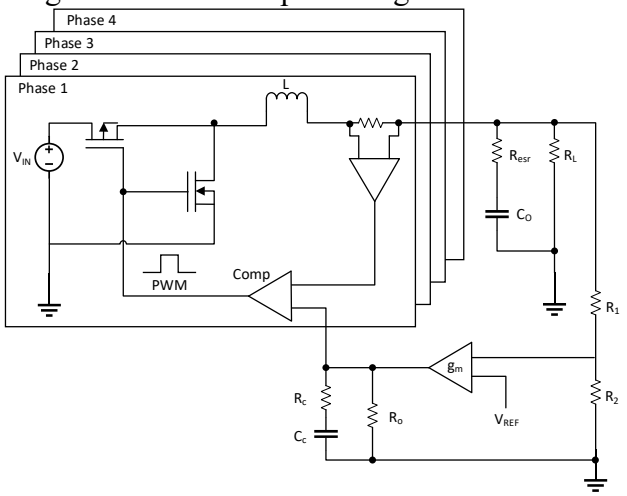


Fig. 1 The Designed Four-phase Parallel Peak Current Mode Controlled DC-DC Converter

Through switch state averaging, the small-signal equivalent circuit of the four-phase DC-DC converter can be drawn as shown in Fig. 2, and its open-loop gain can be expressed as:

$$G_{vd}(s) = \frac{V_{in}(1 + sR_{esr}C_o)}{s^2 \cdot \frac{LC}{4} + s(\frac{L}{4R_L} + R_{esr}C_o) + \frac{R_{esr}}{R_L} + 1}$$

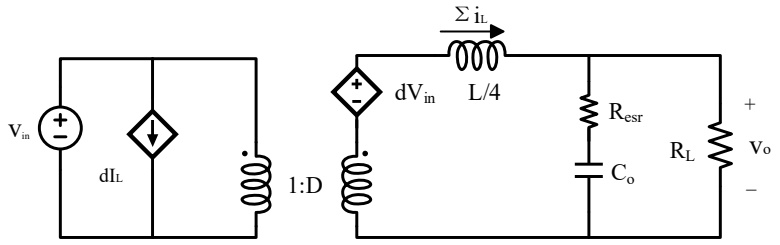


Fig. 2 The small-signal equivalent circuit of the four-phase DC-DC converter

It can be seen that $G_{vd}(s)$ contains a pair of low-frequency conjugate poles and a high-frequency zero, and the Bode diagram is shown in Figure 3.

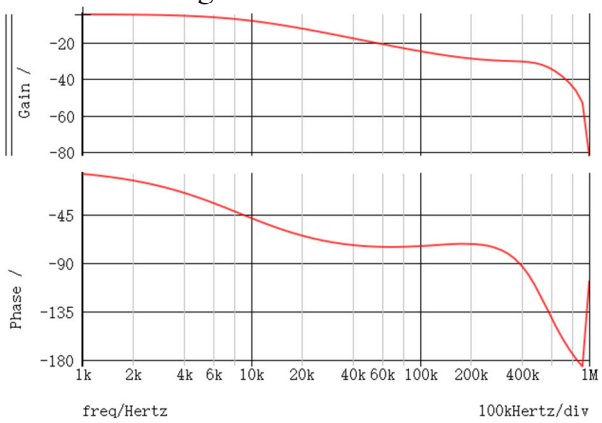


Fig. 3 The open-loop gain of the system before compensation

2.1 Ramp Compensation for Peak Current Control

PCM uses the inductor current waveform instead of the sawtooth wave in voltage-mode control as one input signal of the comparator. Introducing the inductor current as a feedback control variable, fluctuations in the input voltage or load current will cause changes in the inductor current, so PCM has a faster transient response and the ability to automatically limit the current peak. At the same time, PCM also has the problems of inaccurate control of load current and poor anti-interference. Moreover, when D>0.5, the switching converter will produce subharmonic oscillation.

To solve the problem of subharmonic oscillation when D>0.5, this paper superimposes a periodic compensation ramp with a slope of $-m_c$ on the non-inverting input terminal of the comparator. In the BUCK circuit, m_1 and m_2 are the frequencies of the inductor current IL in the rising and falling stages, respectively. Their values are:

$$m_1 = \frac{V_g}{L}, \quad -m_2 = \frac{V_g - V_o}{L}$$

In the range of duty cycle 0≤D<1, to ensure the converter works normally when a is the minimum value, the ramp compensation slope is usually selected as m_c=0. 5m_2. The introduction of the compensation ramp can ensure the stable operation of the PCM switching converter, but it also reduces the dynamic performance of the switching converter.

2.2 Compensation Network Design

The design of the compensation network for the control system is to add a device whose parameters can be adjusted according to actual needs in the system, so that the system characteristics change to meet the given performance indicators of the controlled object. For the power stage circuit of the CCM converter, the transfer function from control to output has two separate poles. Due to the dynamic response, zero-pole compensation can expand the bandwidth and speed up the response, so zero-pole compensation is better than main-pole compensation. In this paper, a Type II error amplifier is used. The compensator has two poles and one zero, and the transfer function can be expressed as:

$$\frac{V_c}{{}^1/_2 V_o} = \frac{1 + sR_5C_2}{sR_3(C_2 + C_3)(1 + sR_5\frac{C_2C_3}{C_2+C_3})}$$

The Type II error amplifier compares the input and output voltage Vo with the reference voltage, and the output compensated error voltage Vc is used as the reference of the current loop to improve the low-frequency high gain to suppress the steady-state error.

The purpose of introducing zeros and poles in the compensator is to cancel the poles and zeros in the control output function. The feedback path of the compensator is composed of a resistor-capacitor series branch to introduce zeros, and a capacitor C_3 is connected in parallel at the output to generate an additional pole. The system zeros and poles can be expressed as:

$$W_{z0}=\frac{1}{C_2R_5},W_{p0}=0,W_{p1}=\frac{C_2+C_3}{C_2C_3R_5}$$

After introducing zeros and poles in the compensator, it will produce a 20dB/dec closed-loop gain response and have sufficient phase margin below the unity gain frequency. To avoid ripple amplification, the design should ensure that the unity gain frequency is lower than $f_{sw}/5$, usually designed at $f_{sw}/10$.

The Bode diagram of the loop gain after compensation is shown in Fig. 4. It can be seen that the crossover frequency is 90kHz, and the phase margin at the crossover frequency is about 40°, so the PCM loop after compensation is stable.

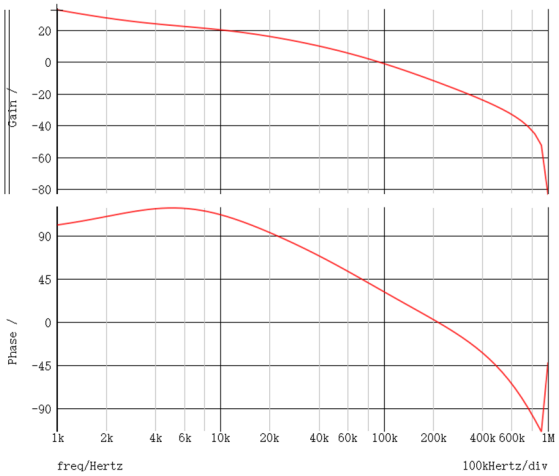


Fig. 4 The open-loop gain of the system after compensation

2.3 Four-Phase PWM Generator

The in-phase terminal of the comparator inputs the inductor current I_{Ln} of each phase, and the reverse terminal inputs the output voltage V_c of the error amplifier. If the reference voltage is greater than V_c, the output voltage of the comparator is positive. Otherwise, the output voltage of the comparator is negative. The output voltage of the comparator is connected to the input terminal of the SR flip-flop.

The four-phase clock signals differ by 90° from each other. Taking Phase1 as an example, when the rising edge of CLK_0 arrives, the SR1 latch is set, so that PWM_1 rises. At this time, the high-side MOS tube of this phase is turned on, and the inductor current IL1 increases linearly until $I_{L1}>V_c$, the comparator outputs 1, the SR_1 latch is reset, and PWM_1 becomes 0, so that the high-side MOS of this phase is turned off, and the inductor current decreases. Thus, the four-phase clock signals set the SR latches in turn to achieve current sharing and determine the duty cycle.

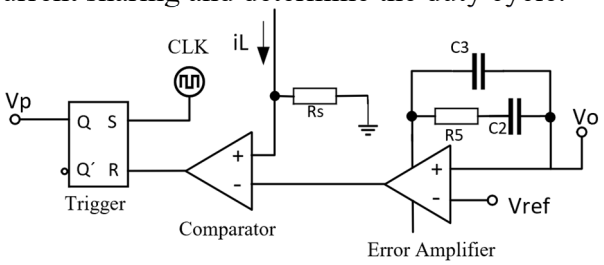


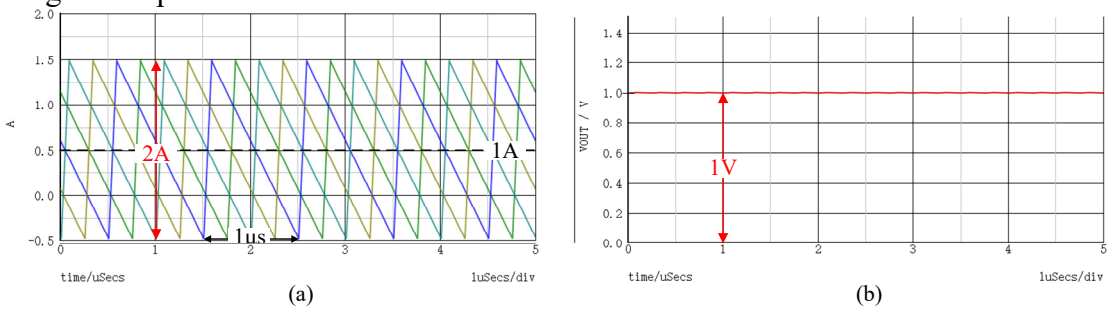
Fig. 5 The four-phase PWM generator

3. Experimental Verification

3.1 Steady-State Test

To verify the steady-state characteristics of the designed peak current mode controlled four-phase DC-DC converter, Simplis simulation verification was carried out on the circuit design. Figs. 6(a)

and (b) show the steady-state inductor current and output voltage waveforms of the designed peak current mode controlled four-phase DC-DC converter, respectively. As can be seen from Fig. 6(a), under steady state, the peak-to-peak value of the inductor current ripple is 2A, and the switching frequency is 1MHz. The inductors of each phase are alternately excited with a 90° phase difference, the current ripples cancel each other out, and the current averages are all equal. As can be seen from Fig. 6(a), under peak current mode control, the output voltage stabilizes at 1V, proving the stability of the designed loop.

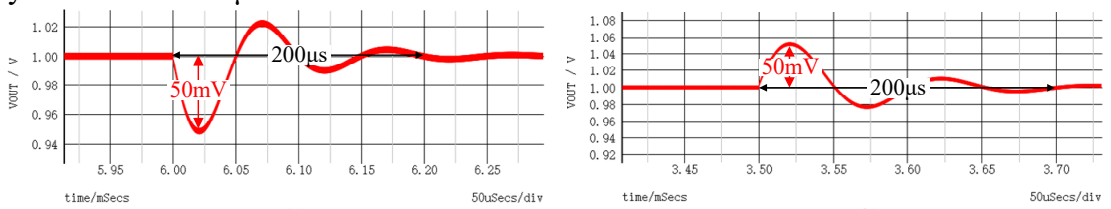


(a) (b)

Fig. 6 The steady-state waveforms of the peak current mode controlled four-phase DC-DC converter:
(a) Inductor current, (b) Output voltage

3.2 Transient Test

To verify the steady-state characteristics of the designed peak current mode controlled four-phase DC-DC converter, Figs. 10(a) and (b) show the output voltage waveforms when the load current jumps up and down by 5A, respectively. As can be seen from Fig. 10(a), for the +5A load current jump, the transient output voltage drop is 50mV, and the recovery time is 200μs. As can be seen from Fig. 10(b), for the -5A load current jump, the transient output voltage overshoot is 50mV, and the recovery time is also 200μs.



(a) (b)

Fig. 7 The transient voltage waveforms of the peak current mode controlled four-phase DC-DC converter:
(a) +5A load current step, (b) -5A load current step.

4. Conclusions

This paper designs and verifies a peak current mode controlled four-phase DC-DC converter. By establishing a small-signal model and optimizing the Type II compensation network, the system achieves a phase margin of 40° at a crossover frequency of 90kHz, ensuring stability. The four-phase PWM is driven in 90° interleaving, the four-phase inductor currents are balanced, and the output voltage error approaches zero. The proposed ramp compensation mechanism eliminates the risk of subharmonic oscillation. Dynamic tests show that under load steps of ±5A, the output voltage overshoot/undershoot is controlled within 50mV, and the recovery time is 200μs. This scheme provides an effective solution for achieving fast transient response requirements.

References

[1] Xiaodong Liu, Changhu Jiang, Yan-Fei Liu and Jiaojiao Deng, "Modeling and analysis of Buck converter based on parallel current mode control strategy," 2009 IEEE 6th International Power Electronics and Motion Control Conference, Wuhan, China, 2009, pp. 500-504.

[2] B. Wang, L. Xian, A. Ukil and H. Beng Gooi, "Approximate-model-based predictive current control for buck converter in CCM," 2017 IEEE Energy Conversion Congress and Exposition (ECCE), Cincinnati, OH, USA, 2017, pp. 5306-5311.

[3] X. Liu, Y. Ye, J. Deng and Y. -F. Liu, "Digital control and simulation of parallel current mode for Buck converter," The 2nd International Symposium on Power Electronics for Distributed Generation Systems, Hefei, China, 2010, pp. 295-298.

[4] P. Roy, K. Banerjee and S. Saha, "Comparison study on the basis of transient response between Voltage Mode Control (VMC) & Current Mode Control (CMC) of buck converter," 2018 International Symposium on Devices, Circuits and Systems (ISDCS), Howrah, India, 2018, pp. 1-4.

[5] Y. -S. Hwang, J. -J. Chen, Y. -T. Ku and J. -Y. Yang, "An Improved Optimum-Damping Current-Mode Buck Converter With Fast-Transient Response and Small-Transient Voltage Using New Current Sensing Circuits," in IEEE Transactions on Industrial Electronics, vol. 68, no. 10, pp. 9505-9514, Oct. 2021.

[6] A. K. Singh, A. Ghoshal and S. Das, "Peak Current Mode Controlled Phase Shifted Multi-Phase Buck Converter for 48V/72V EV Battery Charging," 2024 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES), Mangalore, India, 2024, pp. 1-6.

[7] Y. -S. Hwang, J. -J. Chen, Y. -T. Ku and J. -Y. Yang, "An Improved Optimum-Damping Current-Mode Buck Converter With Fast-Transient Response and Small-Transient Voltage Using New Current Sensing Circuits," in IEEE Transactions on Industrial Electronics, vol. 68, no. 10, pp. 9505-9514, Oct. 2021.

[8] L. Pei, X. Meng and X. Li, "A Novel Digital-Controlled Current-Mode Single-Inductor-Multiple-Output Buck Converter With Individual Output Overload Protection," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 32, no. 5, pp. 957-961, May 2024.