CMOS Transistor Four-Terminal Addressable Multi-Mode Array Testing Circuit

Honghui Zhu*

School of Integrated Circuits, Huazhong University of Science and Technology, Wuhan, China.

u202214302@hust.edu.cn

Abstract. As CMOS technology nodes continue to shrink, non-ideal effects such as Bias Temperature Instability (BTI) and Random Telegraph Noise (RTN) are increasingly compromising the reliability of advanced devices. These time-dependent variabilities (TDVs) can result in threshold voltage drift and degraded circuit performance, necessitating advanced reliability testing solutions. Existing array testing methods often lack the capability for multi-mode characterization and independent substrate addressing. Our four-terminal addressable multi-mode array testing circuit supports multi-mode degradation and characterization at frequencies of up to 1 MHz. In comparison to traditional architectures, our substrate-independent addressing and Force & Sense architecture improve Id accuracy by 56.9% for NMOS and 62.8% for PMOS, providing a robust testing platform for TDV research under bias effects and addressing the demands of real-world circuit operation.

Keywords: CMOS, reliability, array, multi-mode, substrate bias.

1. Introduction

With the ongoing scaling of CMOS technology nodes to 5 nm and below, the intrinsic non-ideal effects of advanced CMOS devices are increasingly prominent, significantly affecting their reliability[1]. These reliability issues primarily manifest in two categories of test metrics: Time Zero Variability (TZV), which reflects inherent random fluctuations during device fabrication, and Time-Dependent Variability (TDV), which characterizes parameter drift that occurs over prolonged operation[2]. Effects such as Bias Temperature Instability (BTI)[3], Random Telegraph Noise (RTN)[4], and Hot Carrier Injection (HCI)[5] can lead to drift in parameters like threshold voltage (Vth), resulting in performance degradation and potential failure[6][7]. Additionally, Time-Dependent Dielectric Breakdown (TDDB) represents a significant reliability challenge, causing hard breakdown (HBD) and soft breakdown (SBD) that can lead to functional failure or increased leakage current[8][9], further exacerbating the randomness and unpredictability of TDV. Stress during the off-state can also degrade circuit performance, potentially interacting with these degradation modes[10][11]. These effects impose stringent requirements on reliability design for devices at advanced process nodes.

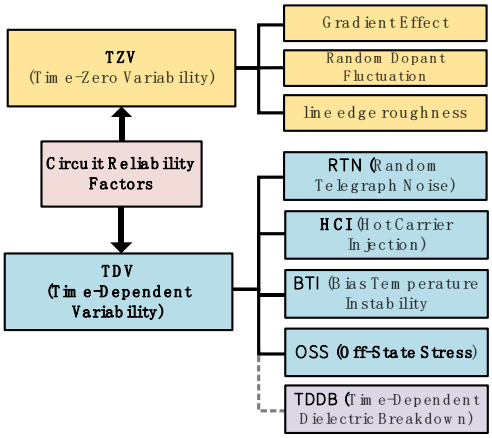

Fig. 1. Current Circuit Reliability Impact Factors

Current research on addressable array testing circuits is summarized in Table I. The Transistor Matrix Array mentioned in [12] and the Addressable Array Test Structure in [13] provide in-depth

studies on RTN characterization. The circuit architectures in [14] and [15] utilize the Measure-Stress-Measure (MSM) method to characterize BTI properties, while [16] offers detailed characterization of RTN and NBTI. Although studies [17] and [10] support TDV characterization in more than three modes, they have limitations: the circuit in [17] lacks TDDB and OSS characterization, while the circuit in [10] does not support TDDB characterization and lacks a Force & Sense architecture. Therefore, the current research landscape exhibits two key characteristics:

Characterization Modes: While characterization testing circuits, excluding TDDB, have been extensively studied, few can perform multi-mode characterization, with most addressing only one or two TDV effects, which is insufficient.

Addressing Methods: Current testing circuits utilize gate and drain addressing, with no circuits available for independent substrate addressing, thereby preventing the characterization of TDV mechanisms under substrate bias effects and failing to meet the demands of real-world circuit operating conditions.

Based on simulations using Virtuoso, our four-terminal addressable multi-mode array testing circuit for CMOS transistors can achieve multi-mode degradation and characterization of RTN, HCI, NBTI, PBTI, TDDB, and OSS at frequencies of up to 1 MHz. It also supports independent substrate addressing for bias operations, establishing a reliable testing platform for TDV research. Furthermore, our circuit provides corresponding CV characterization modes for studying the degradation of MOS device capacitance.

Table 1 Comparison of metrics with other reliability test circuits

	Substrate Addressable	*Process Node*	*Force & Sense*	*HCI*	*PBTI*	*RTN*	*NBTI*	*TDDB*	*OSS*
[12]	×	65nm	✓	×	×	✓	×	×	×
[13]	×	28nm	✓	×	×	✓	×	×	×
[14]	×	28nm	×	×	✓	×	✓	×	×
[15]	×	28nm	×	×	✓	×	✓	×	×
[16]	×	20nm	✓	×	×	✓	✓	×	×
[17]	×	65nm	✓	✓	✓	✓	✓	×	×
[10]	×	?	×	✓	✓	✓	×	×	✓
Our Work	✓	**45nm**	✓	✓	✓	✓	✓	✓	✓

2. Target Function of Our Circuits

Integrating the various TDV degradation modes presented in Fig. 1 with the circuit performance metrics compared in Table I, our circuit design framework is outlined as follows:

Circuit Structure: Develop a circuit capable of supporting independent substrate addressing for bias operations, allowing users to choose whether to address the substrate independently, thereby filling the gap in TDV characterization caused by substrate bias.

Multi-Mode Support: Implement multiple modes, each with a specific port biasing strategy tailored to the TDV modes depicted in Fig. 1, including both NMOS and PMOS devices.

Force & Sense Monitoring: Incorporate a Force & Sense monitoring strategy to ensure high-precision testing requirements.

Characterization Speed: Achieve a characterization speed of up to 1 MHz to satisfy high-speed testing demands.

3. Circuit Design

Our CMOS transistor four-terminal addressable multi-mode array testing circuit will be introduced in four sections. First, the study will outline the overall circuit topology. Next, it will discuss the

design and optimization of the transmission gates. Then, researchers will provide a detailed explanation of the substrate-addressable architecture that supports Force & Sense. Finally, researchers will present the implementation strategy for multi-mode testing.

3.1 Overall Circuit Topology

Fig. 2 illustrates the overall design architecture of the CMOS transistor four-terminal addressable multi-mode array testing circuit. The circuit consists of two main components: a core 32×32 addressable DUT (Device Under Test) array and an array control circuit. This array is divided into 32×16 NMOS DUT units and 32×16 PMOS DUT units. The array control circuit includes an addressing control unit and a test voltage control unit.

External address signals are synchronized through an address buffer before being input to the row and column decoders. Under the control of these decoders, the circuit selects a specific DUT from the 32×32 addressable array for degradation characterization. The NP_EN signal selects the type of DUT, with a high level indicating NMOS and a low level indicating PMOS.

External mode selection signals are synchronized through a test mode buffer before being input to the multi-mode control unit. This unit generates different biasing strategies based on the input mode code. The Mode<2:0> signal is used to select the current degradation and measurement mode, while Bulk_EN facilitates substrate-independent addressing, with a high level indicating independent addressing and a low level indicating source-to-bulk shorting.

External test voltage signals pass through the multi-mode control unit and are then input to the 32×32 addressable DUT array. The voltage is applied to the gate, source, drain, and substrate of the selected DUT unit for degradation characterization. Simultaneously, the 32×32 addressable DUT array outputs a sense voltage to correct for voltage drops caused by the transmission gates, ensuring that the four-terminal stress on the DUT is maintained at ideal values.

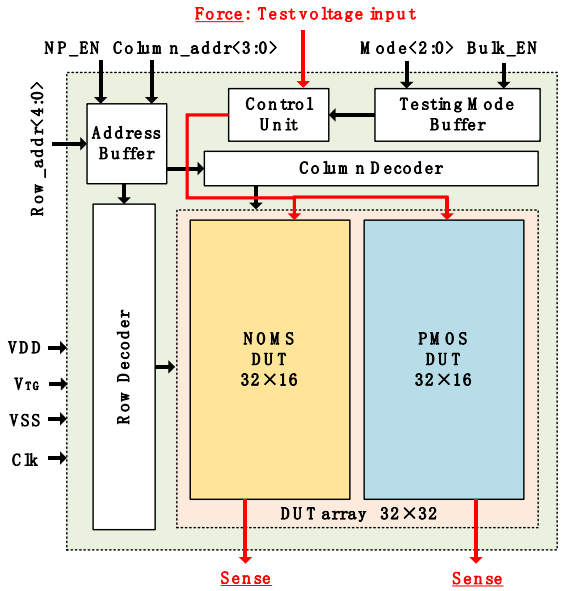

Fig. 2. General architecture of a four-terminal addressable multi-mode array test circuit and connection to external I/O ports

Fig. 3 illustrates the internal connections of the 32×32 addressable DUT array and the control circuit. The Force voltage inputs for each column of DUT units are supplied by the multi-mode control unit. In the figure, red lines indicate the source testing voltage path, blue lines represent the substrate testing voltage path, green lines denote the drain testing voltage path, and black lines indicate the source testing voltage path. This color coding will be consistently used for clarity in understanding and explanation.

The Force voltage output from the multi-mode control unit does not directly affect the DUT. Instead, it first passes through an isolation circuit. If the currently selected address does not

correspond to the DUT, the isolation circuit for that DUT will be disabled, preventing any influence from the test voltage. Conversely, if the current address selects the DUT, the isolation circuit will be activated, applying different input stresses according to the stress and test modes. The specific implementation of the isolation circuit will be detailed in Section C.

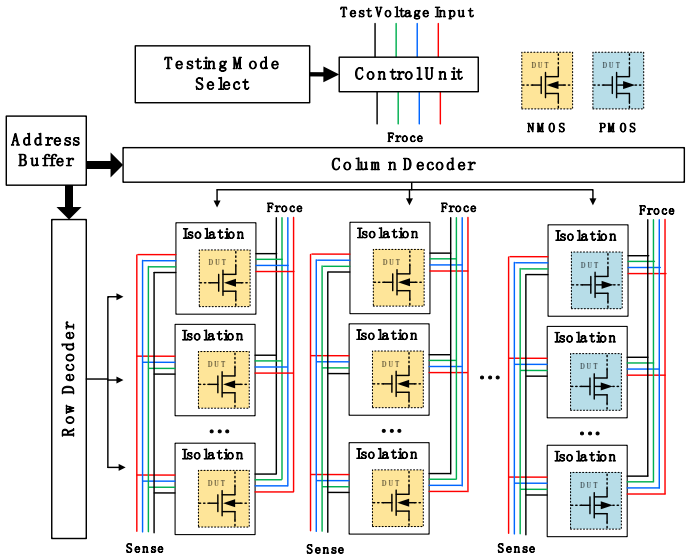

Fig. 3. Internal connections between the 32 x 32 DUT unit array, external test voltage input Control unit, Decoder, Address buffer, and Test mode select

3.2 Transmission Gate Optimization

For a PMOS transmission gate (W/L = 180 nm/50 nm) with its substrate connected to Vdd and an NMOS (W/L = 90 nm/50 nm) with its substrate connected to GND, as shown in Fig. 4(a), the output is in a high-impedance state when the transmission gate (TG) is off, resulting in an unstable output level. When the gate is on, if the input voltage exceeds 1.5 V, a significant voltage drop will occur at the output.

To mitigate the uncertainty of the output voltage when the TG is off, researchers connect a pull-down NMOS to the output, as illustrated in Fig. 4(b). When the transmission gate is off, the output level stabilizes around 0 V. It is important to note that when the input voltage exceeds 1.5 V, the cutoff characteristics of the transmission gate worsen, causing the output voltage to rise significantly above 0 V. However, this error can be corrected in subsequent Force & Sense processing.

To optimize the voltage drop at the output when the TG is on, researchers connect the substrate voltage of the PMOS to 2.5 V instead of Vdd (0.9 V), as shown in Fig. 4(c). This optimization reduces the threshold voltage of the PMOS, thereby lowering its on-resistance and minimizing the voltage drop.

Ultimately, by implementing a pull-down NMOS at the output and connecting the PMOS substrate voltage to 2.5 V, the TG can effectively transmit voltages ranging from 0 to 2.5 V. Additionally, since the required gate voltage is 0 to 2.5 V (VGMAX) for TDDB mode stress, while the source, drain, and substrate voltages required are 0 to 1.5 V (VSMAX, VDMAX, VBMAX) for HCI and BTI modes, researchers conducted different simulations for the isolation of the DUT gate transmission gate (TGF) and the source (TSF), drain (TDF), and substrate (TBF) isolation. As shown in Fig. 4(c) and (d), the non-ideal behaviors of TSF, TDF, and TBF can be completely eliminated, while TGF still exhibits unavoidable errors.

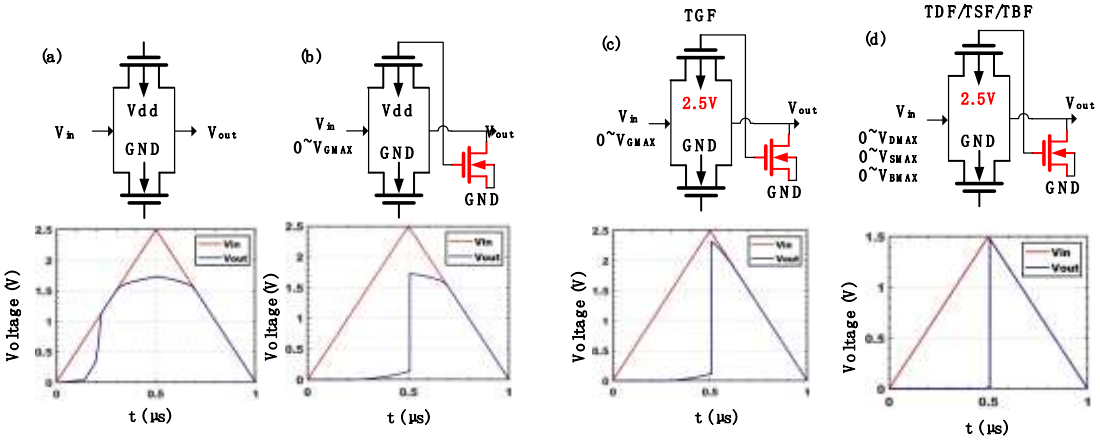

Fig. 4. Input-output characteristics of a transmission gate at cutoff (0-0.5μs) and conduction(0.5-1.0μs). (a) Input-Output Characteristics of a Simple Transmission Gate. (b) Input-Output Characteristics of a Transmission Gate Transmission with a pull-down transistor. (c) Input-output characteristics of a transmission tube with a PMOS substrate bias voltage of 2.5 V and a pull-down transistor, under the input voltage range of 0 to VGMAX. (d) Input-output characteristics of a transmission tube with a PMOS substrate bias voltage of 2.5 V and a pull-down transistor,under the input voltage range of 0 to VDMAX,VSMAX and VBMAX.

3.3 Substrate Addressable Force&Sense Architecture

Circuit simulations indicate that when a specific DUT is selected by the row and column decoders, the voltage drop caused by the isolation circuit is represented by the red line in Fig. 5. This voltage drop closely aligns with the simulation results shown in Fig. 4. Such drops can significantly impact stress testing. Therefore, this paper introduces the Force & Sense architecture to eliminate the voltage drop caused by the isolation circuit.

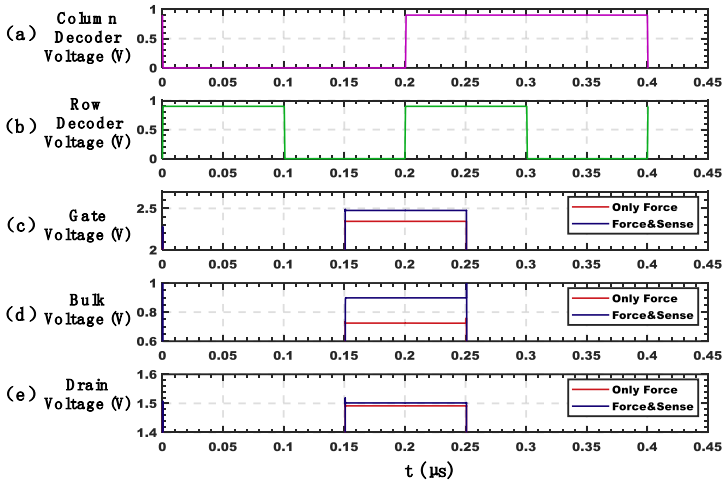

Fig. 5. Stresses in the DUT unit with only Force and with Force&Sense. (a) Column Decoder Voltage. (b) Row Decoder Voltage. (c) Gate Voltage. (d) Bulk Voltage. (e) Drain Voltage.

The Force & Sense architecture supports independent substrate addressing. As shown in Fig. 6(a), in Stress mode, when the DUT is selected, all transmission gates (TGs) are activated. The Force voltage is applied to the DUT's gate, source, drain, and substrate ports, while the Sense pathway connects to external instruments to monitor the voltages at each port in real time, providing feedback to the external input voltage source. Through the feedback adjustment from the Sense feature, all ports of the DUT can achieve ideal voltage values.

As illustrated in Fig. 7, in a state with only Force applied, the voltages at the DUT's ports deviate to varying degrees from their ideal values. However, when employing the Force & Sense architecture with independent substrate addressing, all ports of the DUT can attain the ideal voltage values.

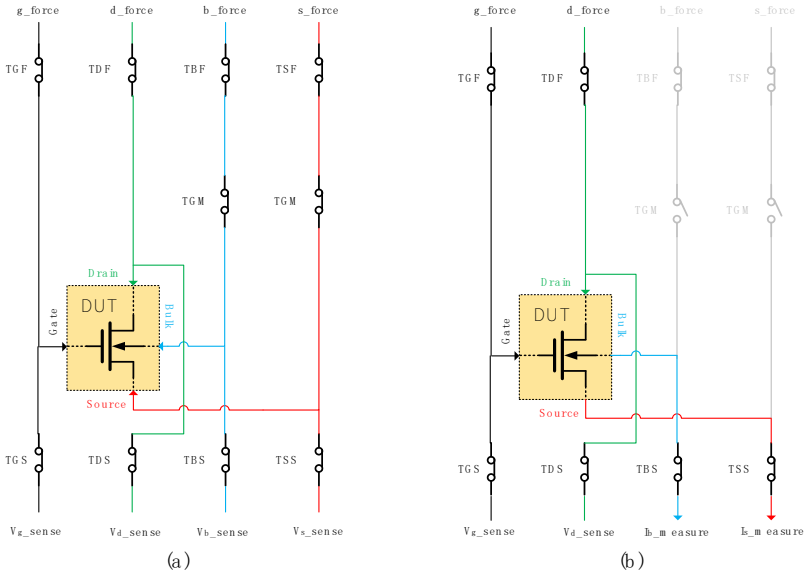

Fig. 6. DUT isolation architecture with Force&Sense support. (a) Force&Sense stress mode. (b) Force&Sense measurement mode.

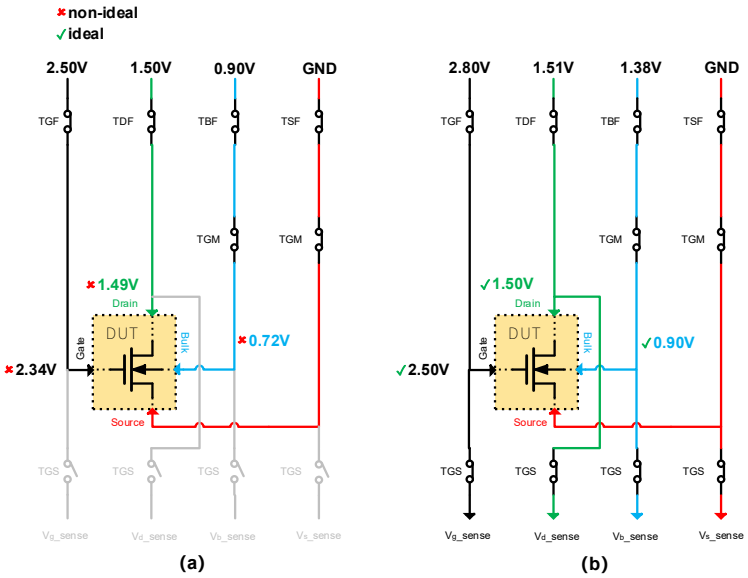

Fig. 7. Stress schematic of the DUT unit (a) Only Force (b) Force&Sense

In Measure mode, as shown in Fig. 6(b), the Transmission Gate for Measure (TGM) located on the source and substrate paths is turned off. Since this TG does not utilize the optimized transmission gate structure depicted in Fig. 4(c) and (d), the source and substrate voltages of the DUT are determined solely by the Sense end voltage when the gate is off. Measure mode requires only the scanning of the DUT's Id-Vgs characteristic curve or gate leakage current; thus, both Vb_sense and Vs_sense are connected to current measurement instruments, with potentials set at 0.9 V (for PMOS) or 0 V (for NMOS). Simultaneously, a normal drain voltage is applied to the d_force terminal, while a test gate voltage ranging from 0 to 0.9 V is gradually increased or decreased at the g_force terminal. The voltages at each port are monitored in real time through the Sense pathway, providing feedback to the d_force and g_force terminals to maintain ideal voltage values. By recording the corresponding source and substrate current values at different Vgs settings, researchers can obtain the Id-Vgs characteristics and gate leakage current curves.

Based on the aforementioned design, Fig. 8 presents the structural diagram of the DUT core unit. The DUT core unit comprises two parts: the DUT itself and its surrounding isolation circuit. This isolation circuit employs the Force & Sense architecture that supports independent substrate addressing, as shown in Fig. 6(a). The elements TGF, TDF, TBF, TSF, TGS, TDS, TBS, and TSS

utilize the optimized transmission gate structure depicted in Fig. 4(c) and (d), while the optimized transmission gate without the pull-down NMOS represents the implementation structure of TGM. The operation of TGF, TDF, TBF, TSF, TGS, TDS, TBS, and TSS is controlled by signals from the row and column decoders synchronized through D flip-flops (DFF), while TGM is controlled by the Measure signal, which is generated by the multi-mode control unit.

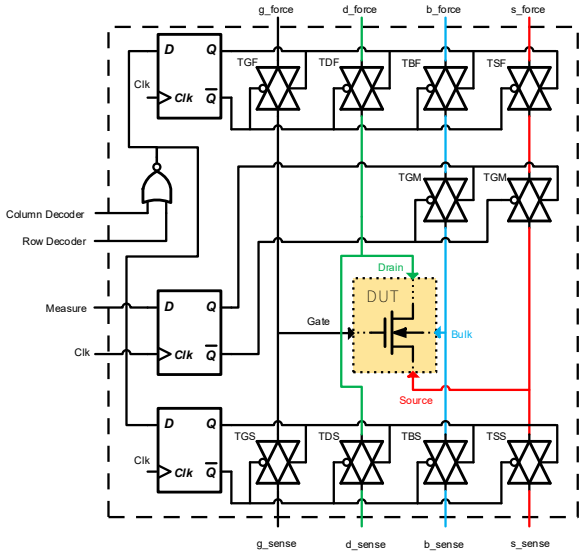

Fig. 8. Four-terminal addressable Force&Sense architecture

3.4 Multi-mode Test Design

This section outlines the implementation strategy for multi-mode testing. According to the design objectives, the system configures various testing modes and corresponding electrical biasing methods using mode control codes (as shown in Table 2). When the mode code is set to 000 (Measure mode), the system disables the TGM in the DUT isolation module and measures the source-drain current and gate leakage current after applying stresses from HCI, PBTI, NBTI, off-state stress, and TDDB. For mode codes 001 (HCI stress mode), 010 (TDDB, PBTI, NBTI stress mode), 110 (off-state stress mode), and 111 (MOS capacitor mode), the system applies the appropriate test voltages specified in Table 2 for each degradation mode.

When Bulk_EN is set to 0, both the substrate and source terminals are connected to GND (for NMOS) or VDD (for PMOS), indicating that the substrate is not independently addressed. When Bulk_EN is set to 1, both the substrate and source terminals are connected to an external test voltage input, enabling independent stress on the source and substrate.

Table 2 Degradation modes corresponding to different mode select bits

Select bits		*Test Mode(Stress&Measure)*	*g_out*	*d_out*	*b_out*	*s_out*	
Bulk_EN	**Mode<2:0>**					NMOS	PMOS
0	000	*Initial, RTN, HCI, PBTI, NBTI, off-state*	*g_in*	*d_in*	***s***	*GND*	V_{dd}
	001	*HCI*	*g_in*	*d_in*			
	010	*TDDB, PBTI, NBTI*	*g_in*	***s***			
	110	*off-state*	GND/V_{dd}	*d_in*			
	111	*Capacitance*	*g_in*	***s***	*b_in*		
1	000	*Initial, RTN, HCI, PBTI, NBTI, off-state*	*g_in*	*d_in*		*GND*	V_{dd}
	001	*HCI*	*g_in*	*d_in*		*s_in*	
	010	*TDDB, PBTI, NBTI*	*g_in*	***s***	*b_in*		
	110	*off-state*	GND/V_{dd}	*d_in*			
	111	*Capacitance*	*g_in*	***s***			

To implement the control relationships outlined in Table 2, researchers utilize the structure shown in Fig. 9. External test mode selection signals are synchronized through a multi-mode test buffer before being input to the multi-mode control unit. Mode<2:0> is first decoded by a 3-to-8 decoder into five test mode enable signals (active low). These enable signals, along with NP_EN and Bulk_EN, are input to the control core, which manages the on/off states of the TGs on the source, drain, and substrate paths, determining whether the test voltage applied to the DUT ports is Vdd, GND, or an external voltage. The input-output control logic of the multi-mode control unit is illustrated in Fig. 10. The enable signal for mode 000 generated by the 3-to-8 decoder will directly serve as the Measure signal for each DUT isolation unit, controlling the activation of the TGM.

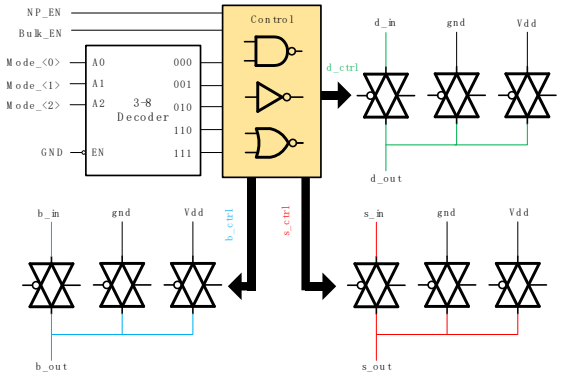

Fig. 9. Architecture of the Multi-Mode Control Unit

Fig. 10 details the voltage biasing strategies of the multi-mode control unit under four configurations: NMOS standard addressing (NP_EN = 1, Bulk_EN = 0), PMOS standard addressing (NP_EN = 0, Bulk_EN = 0), NMOS substrate addressing (NP_EN = 1, Bulk_EN = 1), and PMOS substrate addressing (NP_EN = 0, Bulk_EN = 1). Each mode encompasses five mode codes (000, 001, 010, 110, 111), representing stresses or characterizations under different degradation conditions. The first six entries in the logic table correspond to the control signals of the multi-mode control unit, while the last three indicate the voltage outputs for the drain, substrate, and source, covering all circuit modes.

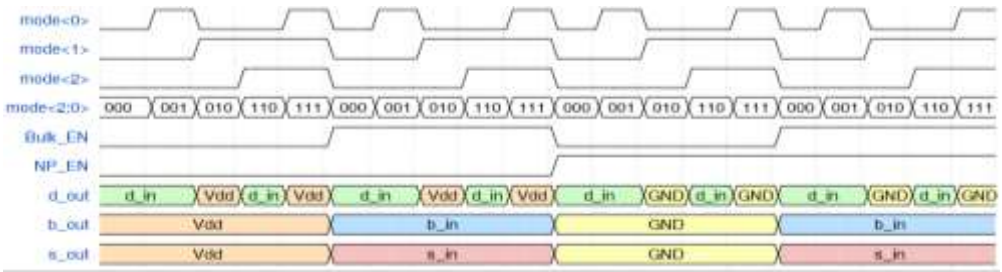

Fig. 10. Control Logic for Multi-Mode Control Unit

4. Resluts

To evaluate the performance of the CMOS transistor four-terminal addressable multi-mode array testing circuit, researchers conducted comprehensive simulations using Virtuoso. First, the study performed a standalone simulation of the Measure mode and compared the results with the ideal scenario. Next, researchers simulated the actual testing process for the DUT, conducting a multi-mode joint simulation of the DUT's biasing conditions. The simulation results indicate that the circuit effectively meets the requirements for both Measure and Stress modes.

4.1 Measure Mode Results

In Measure mode, this study conducted three simulations for both NMOS and PMOS DUTs. Researchers scanned the DUT's Id-VGS curve under conditions with only Force applied and with both Force and Sense feedback, comparing these results to those obtained from a direct scan of the DUT.

Specifically, the study performed three sets of comparative simulations for the NMOS and PMOS DUTs: one where only the Force signal was applied to scan the Id-VGS characteristic curve, another where Sense feedback was introduced while applying the Force signal, and a direct scan of the DUT's Id-VGS characteristic curve. By comparing the simulation results of these three configurations, researchers can assess the impact of Force & Sense on the accuracy of the testing circuit.

The simulation results are presented in Fig. 11 and Fig. 12. For the Id-VGS characteristic curve of the NMOS (W/L = 90 nm/50 nm), the maximum current error reached 56.9% compared to the ideal case when only the Force signal was applied. For the PMOS (W/L = 90 nm/50 nm), the maximum current error was 62.8%. However, after introducing Sense feedback, the simulation results showed that the Id-VGS characteristic curves for both NMOS (W/L = 90 nm/50 nm) and PMOS (W/L = 90 nm/50 nm) closely aligned with the ideal curves, indicating that the circuit operated correctly in Measure mode.

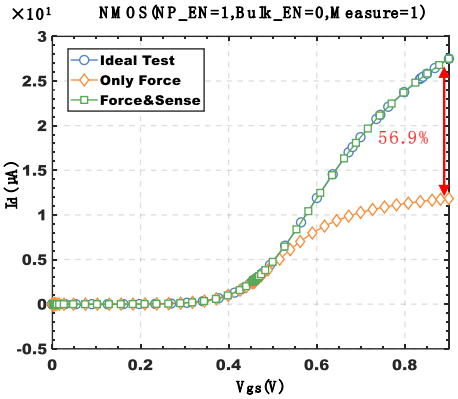

Fig. 11. Id-Vgs Characteristics of NMOS in the Ideal Case, Force Only Case and Force&Sense Case

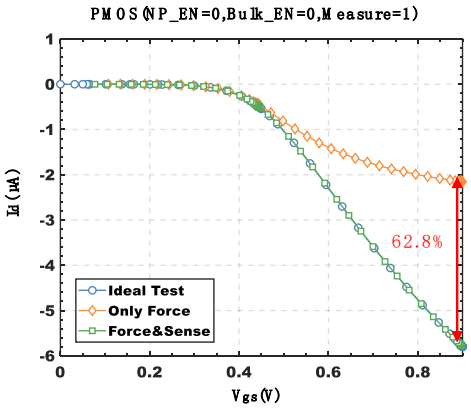

Fig. 12. Id-Vgs Characteristics of PMOS in the Ideal Case, Force Only Case and Force&Sense Case

4.2 Multi-mode Stress Results

To assess whether the circuit operates correctly under various modes, researchers simulated the actual DUT testing process by applying bias in the following sequence: Initial, RTN, HCI stress, HCI measurement, BTI (with PBTI measured when NP_EN=1 and NBTI when NP_EN=0), BTI measurement, off-state stress, off-state measurement, TDDB stress, TDDB measurement, and MOS capacitor testing. Researchers conducted real-time monitoring of the gate, source, drain, and substrate voltages under four configurations: NMOS standard addressing, PMOS standard addressing, NMOS

substrate addressing, and PMOS substrate addressing, producing the simulation waveforms illustrated in Fig. 13.

From Fig. 13, it is evident that in standard addressing mode (Bulk_EN=0), during the Initial, RTN, HCI measurement, BTI measurement, off-state measurement, and TDDB measurement modes (000), |VGS| can be scanned from 0 to 0.9 V, and |VDS| can be applied at normal operating voltage. In HCI stress mode (001), both |VGS| and |VDS| can reach 1.5 V. In BTI stress mode (010), |VGS| can achieve 1.5 V while |VDS| is maintained at 0 V. In off-state stress mode (110), |VDS| can reach 1.5 V with |VGS| at 0 V. In TDDB stress mode (010), |VGS| can reach 2.5 V while |VDS| remains at 0 V. In MOS capacitor mode (111), |VGB| can reach 0.6 V, while |VDS| stays at 0 V.

When researchers set Bulk_EN to 1, the system enters substrate addressing mode, allowing for external application of substrate bias to the DUT. As shown in Fig. 13(c) and (d), while maintaining the standard addressing bias state, the circuit can apply a substrate bias voltage |VGB| ranging from 0 to 1.5 V, enabling the investigation of the device's TDV characteristics under the influence of substrate bias.

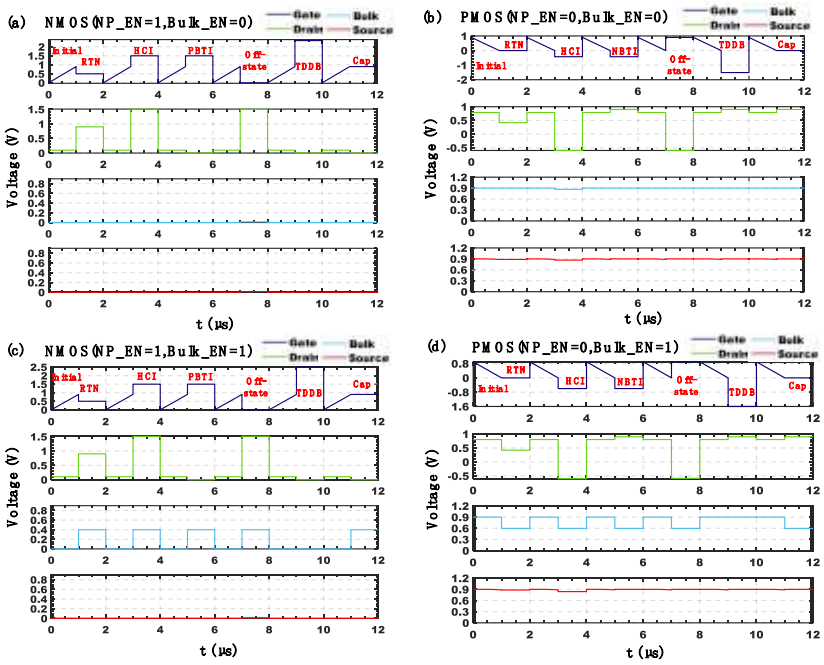

Fig. 13. Full-flow stressing and measurement with independent substrate addressing. (a) NMOS Standard Addressing (NP_EN=1, Bulk_EN=0) (b) PMOS Standard Addressing (NP_EN=1, Bulk_EN=0) (c) NMOS Substrate Addressing (NP_EN=0, Bulk_EN=1) (d) PMOS Substrate Addressing (NP_EN=0, Bulk_EN=1)

5. Conclusions

The CMOS transistor four-terminal addressable multi-mode array testing circuit presented in this study supports the testing of various reliability degradation mechanisms, enabling the characterization of RTN, HCI, BTI, TDDB, and OSS. The circuit can apply a maximum |VDS| of 1.5 V and a maximum |VGS| of 2.5 V, while also facilitating CV characterization of MOS device capacitance degradation. Additionally, the circuit achieves a maximum testing frequency of 1 MHz, fulfilling the requirements for high-speed reliability testing.

By utilizing a Force & Sense architecture with independent substrate addressing, the testing accuracy is significantly improved compared to traditional methods that apply only Force voltage. For NMOS (W/L = 90 nm/50 nm) and PMOS (W/L = 90 nm/50 nm) devices, the testing accuracy increases by 56.9% and 62.8%, respectively. Furthermore, the unique substrate independent addressing and biasing capability of this architecture provides a reliable platform for investigating TDV characteristics under substrate bias effects.

6. References

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